WHAT IS CLAIMED IS:

1. An output circuit for outputting data with reduced simultaneous switching output skew, said output circuit comprising:

N counts of output buffers receiving N counts of bit signals, respectively, at least one of said output buffers comprising a delay unit for processing one of said bit signals into a delayed bit signal with an adjustable delay period in response to a delay signal, a pull-up unit electrically connected to said delay unit and a source voltage, and selectively enabled to output said delayed bit signal as a high level, and a pull-down unit electrically connected to said delay unit and a ground voltage, and selectively enabled to output said delayed bit signal as a low level; and

a comparator in communication with said N counts of output buffers, comparing said N counts of bit signals sampled at a first time spot and a second time spot, and generating said delay signal according to the comparing result.

2. The output circuit according to claim 1 wherein said delay signal is at a first logic state when a first number of said output buffers changing from said high level to said low level at output terminals thereof between said first and said second time spots is larger or less than a second number of said output buffers changing from said low level to said high level to a predetermined extent, and said delay signal is at a second logic state level when the difference between said first and said second numbers is within a specified range.

3. The output circuit according to claim 2 wherein said comparator further generates a control signal which is at said first logic state when said first number is smaller than said second number, and at said second logic state when said first number is larger than said second number.

4. The output circuit according to claim 3 wherein said first logic state is logic

high and said second logic state is logic low.

5. The output circuit according to claim 3 wherein said delay unit comprises:

an adder/subtractor electrically connected to said comparator, performing an adding operation of said delay signal with a preset value when corresponding one of said bit signals is at said high level and said control signal is at said low logic state, or when said corresponding one of said bit signals is at said low level and said control signal is at said high logic state, and performing a subtracting operation of said delay signal with said preset value when said corresponding one of said bit signals and said control signal are both logic high or both logic low; and

a delay adjusting circuit electrically connected to said adder/subtractor, processing said corresponding one of said bit signals into said delayed bit signal with a certain delay period according to the result of said adding operation or said subtracting operation.

6. The output circuit according to claim 5 wherein said certain delay period is a basic delay period if the result of said adding or subtracting operation is equal to said preset value, said certain delay period is longer than said basic delay period when the result of said adding or subtracting operation is greater than said preset value, and said certain delay period is shorter than said basic delay period when the result of said adding or subtracting operation is smaller than said preset value.

7. The output circuit according to claim 5 wherein said delay adjusting circuit comprises:

a plurality of buffers electrically interconnected in series, differentially imparting said corresponding one of said bit signals with a plurality of delay periods, respectively; and

a multiplexer electrically connected to said adder/subtractor and said plurality of buffers, selecting one of said plurality of delay periods as said certain delay period in response to a select signal correlating to the result of said adding operation or said subtracting operation.

8. An output circuit for outputting data with reduced simultaneous switching output skew, said output circuit comprising:

N counts of output buffers receiving N counts of bit signals, respectively, comprising at least two delay units for processing two of said bit signals into a first and a second delayed bit signals with a first and a second delay periods, respectively, in response to a delay signal, wherein said first and said second delay periods are different in a first situation and identical in a second situation; and

a comparator in communication with said N counts of output buffers, comparing said N counts of bit signals sampled at a first time spot and a second time spot, and generating said delay signal according to the comparing result.

9. The output circuit according to claim 8 wherein said first situation stands when the number of said output buffers changing from the high level to the low level at output terminals thereof between said first and said second time spots is larger than that changing from the low level to the high level to a predetermined extent.

10. The output circuit according to claim 8 wherein said first situation stands when the number of said output buffers changing from the high level to the low level at output terminals thereof between said first and said second time spots is less than that changing from the low level to the high level to a predetermined extent.

11. The output circuit according to claim 8 wherein said second situation stands

when the difference of the number of said output buffers changing from the high level to the low level at output terminals thereof between said first and said second time spots and that changing from the low level to the high level is within a specified range.

12. The output circuit according to claim 8 wherein said second situation stands when all said N counts of output buffers change from the high level to the low level at output terminals thereof between said first and said second time spots.

13. The output circuit according to claim 8 wherein said second situation stands when all said N counts of output buffers change from the low level to the high level at output terminals thereof between said first and said second time spots.

14. The output circuit according to claim 8 wherein said output buffers further comprise:

a pull-up unit electrically connected to one of said delay units and a source voltage, and enabled to output corresponding one of said first and said second delayed bit signals as the high level; and

a pull-down unit electrically connected to the other one of said delay units and a ground voltage, and enabled to output the other one of said first and said second delayed bit signals as the low level.

15. A method for outputting data with reduced simultaneous switching output skew, comprising steps of:

comparing bit signals sampled at a current time spot with those sampled at a preceding time spot to obtain a first number of said bit signals changing from the high level to the low level and a second number of said bit signals changing from the low level to the high level;

comparing said first number with said second number to obtain a first comparing result, and asserting a delay control signal according to said first

comparing result;

processing each of said bit signals into a delayed bit signal with a certain delay period, wherein said certain delay period is determined by said delay control signal; and

outputting each said delayed bit signal.

16. The method according to claim 15 further comprising steps, before outputting each said delayed bit signal, of pulling up said delayed bit signal when said delay bit signal is at the high level, and pulling down said delayed bit signal when said delay bit signal is at the low level.

17. The method according to claim 15 wherein said delay control signal includes a delay signal for delaying any of said bit signals changing from the high level to the low level with a first delay period, and delaying any of said bit signals changing from the low level to the high level with a second delay period, and wherein said second delay period is different from said first delay period when the difference between said first number and said second number is beyond a preset range.

18. The method according to claim 17 wherein said first delay period is longer than said second delay period when said first number is smaller than said second number, and said first delay period is shorter than said second delay period when said first number is larger than said second number.

19. The method according to claim 17 wherein said second delay period is equal to said first delay period when the difference between said first number and said second number is within a preset range.

20. The method according to claim 17 wherein said delay control signal includes a control signal being a first logic state when said first number is larger than said second number, and a second logic state when said first number is

smaller than said second number.

21. The method according to claim 20 wherein said step of processing each of said bit signals comprises sub-steps of:

determining which one of an adding operation and a subtracting operation is performed for one of said bit signals with high/low level change and said control signal;

performing said adding operation or said subtracting operation of said delay signal with a preset value to obtain an operational result;

comparing said operational result with said preset value to obtain a second comparing result;

selecting one of a plurality of preset delay periods as said first delay period or said second delay period according to said second comparing result; and

delaying said one of said bit signals with said first or said second delay period.